CLAIMS

What is claimed is:

1. A method of flashing an image to a plurality of electrically erasable programmable read only memories (EEPROMs) across a communication bus, the method comprising:

compressing the image to create a compressed image;

broadcasting the compressed image to the plurality of EEPROMs substantially simultaneously across the communication bus; and

flashing the image onto each of the plurality of EEPROMs.

2. The method of flashing a plurality of EEPROMs as defined in claim 1 wherein compressing the image further comprises:

creating an initial frequency table of an initial image placed on the plurality of EEPROMs; and

creating the compressed image using the initial frequency table.

3. The method of flashing a plurality of EEPROMs as defined in claim 2 further comprising refraining from broadcasting the initial frequency table along with the compressed image.

4. The method of flashing a plurality of EEPROMs as defined in claim 2 wherein creating the compressed image further comprises Huffman encoding.

5. The method of flashing a plurality of EEPROMs as defined in claim 1 wherein broadcasting the image further comprises:

sending the compressed image in a plurality of broadcast packets;

querying each of the plurality of EEPROMs for a list of missing packets from the compressed image; and

broadcasting the missing packets.

6. The method of flashing a plurality of EEPROMs as defined in claim 1 wherein flashing the image onto each of the plurality of EEPROMs further comprises:

flashing the image onto each of the plurality of EEPROMs individually; and

refraining from flashing a remaining EEPROM if any of the plurality of EEPROMs fail to properly flash.

7. The method of flashing a plurality of EEPROMs as defined in claim 1 wherein broadcasting the compressed image further comprises broadcasting the compressed image across a low bandwidth communication bus.

8. A system comprising:

a communication bus;

a first computer system coupled to the communication bus;

a plurality of computer systems coupled to the first computer system across the communication bus, each of the plurality of computer systems having an electrically erasable programmable read only memory (EEPROM) device having an image thereon; and

wherein the first computer system is adapted to simultaneously broadcast a new EEPROM image to each of the plurality of computer systems across the communication bus, the new EEPROM image to be placed in the EEPROM device of each of the plurality of computer systems.

9. The system as defined in claim 8 wherein the first computer system is adapted to compress the new EEPROM image prior to its broadcast.

10. The system as defined in claim 9 wherein the first computer system is adapted to Huffman encode the new EEPROM image prior to its transfer, and wherein the first computer system is further adapted to not send the frequency table used for Huffman encoding along with the new EEPROM image.

11. The system as defined in claim 10 wherein the first computer system uses a predefined frequency table to encode each new EEPROM image.

12. The system as defined in claim 10 wherein the plurality of computer systems each uses a predefined frequency table to decode each new EEPROM image prior to flashing.

13. The system as defined in claim 8 wherein each of the plurality of computer systems further comprises:

a microprocessor coupled to the EEPROM device; and

a random access memory array (RAM) coupled to the microprocessors;

wherein the microprocessor is adapted to receive the new EEPROM image broadcast across the communication bus and store the new EEPROM image in the RAM; and

wherein the microprocessor is further adapted to flash the new EEPROM image to the EEPROM after the entire new EEPROM image is stored in the RAM.

14. The system as defined in claim 13 wherein the first computer system is adapted to compress the new EEPROM image prior to its broadcast.

15. The system as defined in claim 14 wherein the microprocessor of each of the plurality of computer systems is further adapted to decompress the new EEPROM image prior to flashing that new EEPROM image to the EEPROM device.

16. The system as defined in claim 8 wherein each of the plurality of computer systems further comprises:

a microcontroller coupled to the EEPROM device;

a random access memory array (RAM) coupled to the microcontroller;

wherein the microcontroller is adapted to receive the new EEPROM image broadcast across the communication bus and store that image in the RAM; and

wherein the microcontroller is further adapted to flash the new EEPROM image to the EEPROM after the entire new EEPROM image is stored in the RAM.

17. The system as defined in claim 16 wherein the first computer system is adapted to compress the new EEPROM image prior to its broadcast.

18. The system as defined in claim 17 wherein the microcontroller of each of the plurality of computer systems is further adapted to decompress the new EEPROM image prior to flashing that new EEPROM image to the EEPROM device.

19. The system as defined in claim 8 wherein the communication bus further comprises a low bandwidth communication bus.

20. A method of flashing a single image to a plurality of electrically erasable programmable read only memories (EEPROMs) across a communication bus, the method comprising:

sending the single image across the communication bus to each of the plurality of EEPROMs substantially simultaneously; and

flashing the image onto each of the plurality of EEPROMs.

21. The method of flashing a plurality of EEPROMs as defined in claim 20 wherein sending the single image to each of the plurality of EEPROMs substantially simultaneously further comprises broadcasting the single image across the communication bus being a low bandwidth communication bus.

22. The method of flashing a plurality of EEPROMs as defined in claim 20 further comprising, prior to the sending step, compressing the single image to create a compressed single image.

23. The method of flashing a plurality of EEPROMs as defined in claim 22 wherein the sending step further comprises sending the compressed single image across the communication bus to each of the plurality of EEPROMs substantially simultaneously.

24. The method of flashing a plurality of EEPROMs as defined in claim 23 wherein sending the compressed single image to each of the plurality of EEPROMs substantially simultaneously further comprises broadcasting the compressed single image across the communication bus being a low bandwidth communication bus.

25. The method of flashing a plurality of EEPROMs as defined in claim 22 wherein compressing the single image further comprises:

creating an initial frequency table of an initial image placed on the plurality of EEPROMs; and

creating the compressed single image using the initial frequency table created for the initial image.

26. The method of flashing a plurality of EEPROMs as defined in claim 25 further comprising refraining from broadcasting the initial frequency table along with the compressed single image.

27. The method of flashing a plurality of EEPROMs as defined in claim 25 wherein creating the compressed single image further comprises Huffman encoding the single image using the initial frequency table.

28. The method of flashing a plurality of EEPROMs as defined in claim 20 wherein sending the single image further comprises:

sending the single image in a plurality of broadcast packets;

querying each of the plurality of EEPROMs for a list of missing packets from the single image; and

broadcasting the missing packets from the single image.

29. The method of flashing a plurality of EEPROMs as defined in claim 20 wherein flashing the single image onto each of the plurality of EEPROMs further comprises:

flashing the single image onto each of the plurality of EEPROMs individually; and

refraining from flashing a remaining EEPROM if any of the plurality of EEPROMs fail to properly flash.

30. The method of flashing a plurality of EEPROMs as defined in claim 20 wherein sending the single image further comprises sending the single image across a low bandwidth communication bus.

31. A rack mounted computer system comprising:

a first chassis having a plurality of servers mounted therein;

a second chassis having a plurality of servers mounted therein;

a central power supply system coupled to the first and second chassis and supplying power thereto;

a first chassis communication module coupled to each server in the first chassis by way of a first communication bus;

a second chassis communication module coupled to each server in the second chassis by way of a second communication bus;

a third communication bus coupling the first and second chassis communication module;

wherein the first chassis communication module comprises:

a microcontroller coupled to the first communication bus and the third communication bus; and

an electrically erasable programmable read only memory (EEPROM) coupled to the microcontroller and adapted to store software images executed by the microcontroller;

wherein the second chassis communication module comprises:

a microcontroller coupled to the second communication bus and the third communication bus; and

an EEPROM coupled to the microcontroller adapted to store software images executed by the microcontroller;

wherein a server of the plurality of servers in one of the first and second chassis is adapted broadcast simultaneously a new software image to be flashed to each EEPROM in each of the first and second chassis communication modules.

32. The rack mounted computer system as defined in claim 31 wherein the server of the plurality of servers is configured to compress the new software image prior to broadcasting the new software image.

33. The rack mounted computer system as defined in claim 32 further comprising:

said server of the plurality of servers is configured to use Huffman encoding to compress the new software image; and

wherein the first server of the plurality of servers is configured to not send a frequency table used for the Huffman encoding along with the new compressed software image.

34. The rack mounted computer system as defined in claim 33 wherein the server of the plurality of servers is further configured to perform the Huffman encoding using a frequency table that is not specifically indicative of the frequency of symbols in the new software image.

35. The rack mounted computer system as defined in claim 33 wherein each of the microcontrollers in each of the first and second chassis communication modules is adapted to use a predefined frequency table to decompress the new software image prior to flashing.

36. The rack mounted system as defined in claim 31 wherein the first communication bus is a low bandwidth communication bus.

37. The rack mounted system as defined in claim 36 wherein the low bandwidth communication bus is an I^2C serial bus.

38. The rack mounted system as defined in claim 31 wherein the second communication bus is a low bandwidth communication bus.

39. The rack mounted system as defined in claim 38 wherein the low bandwidth communication bus is an I^2C serial bus.

40. The rack mounted system as defined in claim 31 wherein the third communication bus is an RS-485 compliant bus.

41. A system comprising:

a first computer means for sending a new software image;

a plurality of computer means for receiving the new software image, each of the plurality of computer means having an electrically erasable programmable read only memory (ROM) device requiring a software image;

a communication bus means coupling the first computer means and the plurality of computer means, the communication bus means for allowing the first computer means to send the new software images to the plurality of computer means; and

wherein the first computer means is adapted to simultaneously broadcast the new software image to each of the plurality of computer means across the communication means, the new software image to be placed in the EEPROM device of each of the plurality of computer means.

42. The system as defined in claim 41 wherein the first computer means is adapted to compress the new software image prior to its broadcast across the communication means.

43. The system as defined in claim 42 wherein the first computer means is adapted to Huffman encode the new software image prior to its transfer, and wherein the first computer means is further

adapted to not send the frequency table used for Huffman encoding along with the new software image.

44. The system as defined in claim 43 wherein the first computer means uses a predefined frequency table to encode each new software image.

45. The system as defined in claim 43 wherein the plurality of computer means each uses a predefined frequency table to decode each new software image prior to flashing.

46. The system as defined in claim 41 wherein each of the plurality of computer means further comprises:

a digital computing means for executing software programs, the digital computing means coupled to the EEPROM device; and

a memory means for temporarily storing data and software programs, the memory means coupled to the digital computing means;

wherein the digital computer means is adapted to receive the new software image broadcast across the communication means and store the new software image in the memory means; and

wherein the digital computing means is further adapted to flash the new software image to the EEPROM after the entire new software image is stored in the memory means.

47. The system as defined in claim 46 wherein the first computer means is adapted to compress the new software image prior to its broadcast.

48. The system as defined in claim 47 wherein the digital computing means of each of the plurality of computer means is further adapted to decompress the new software image prior to flashing that new software image to the EEPROM device.

49. The system as defined in claim 47 wherein the digital computing means further comprises a microcontroller.

50. The system as defined in claim 47 wherein the memory means further comprises a random access memory array.

51. The system as defined in claim 47 wherein the communication means further comprises a serial communication bus.

52. The system as defined in claim 51 wherein the serial communication bus further comprises an I^2C serial bus.